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USE FIELD-PROGRAMMABLE GATE ARRAY FOR FORMATION OF TEST SIGNAL IMPEDANCE METER

V.A.Kolesnikov, Ya.Zh.Baisagov

Karaganda State University named after E.A. Buketov, Universitetskaya Str.28, Karaganda, 100026, Kazakhstan
kolesnikov.vladimir@gmail.com

This article describes a method of generating test signals for bridge impedance meter with modern high-speed components . The article made rationale for selecting the measuring circuit. The choice of the main hardware components. Describes a method to accomplish the task with the use of a programmable logic array. In operation, is implemented the algorithm programmable logic array in the language of Verilog. There are examples of programs. The result has been designed digital test signal generator for impedance meter.

Keywords: programmable integrated circuit, algorithm, measuring and equivalent circuits, schematic diagram, software module, digital circuit.

As in any modern meter in impedance bridge measurement process must be automated. To impedance bridge meter bridge balancing the need to automate and choice of measurement ranges[1-5].

This article describes a method of forming the test signals for the impedance bridge meter with modern high-speed components such as high-speed digital-to-analog converters (DACs) and Field-Programmable Gate Array (FPGAs).

The objectives of the work described in this article are:

1. Selecting the measuring circuit;
2. DAC chip select;
3. Selecting FPGA;
4. Developing an algorithm of FPGA;
5. Implementation algorithm in Verilog HDL.

Measurement scheme must meet the following requirements:

- wide range of measurements;
- bridge measurement method;
- linearity;
- ease of calibration;

Satisfies these requirements meter bridge circuit shown in Figure 1. This circuit consists of two alternating current sources of equal frequency G1 and G2, measured resistance Rx, reference resistance R0, and the zero detector ZD.

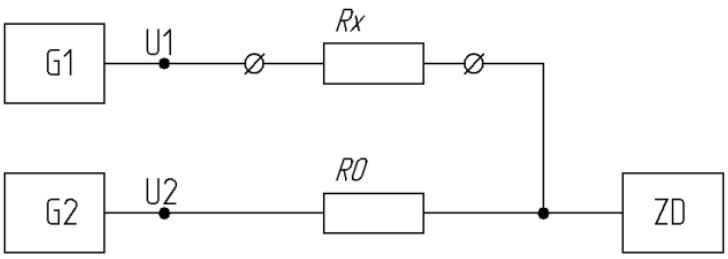

Fig.1. Measuring curcut.

AC source G1 generates sinusoidal alternating voltage constant frequency amplitude and phase. G2 voltage source generates a frequency the same as G1. Phase and amplitude of the signal source G2 can vary over a wide range. When both legs of circuit are balanced , voltage detector zero ZD takes close to zero voltage. The equivalent circuit is shown in Figure 2. In this scheme, it is clear that to achieve the balance of the bridge is necessary that the currents i1 and i2 are equal.

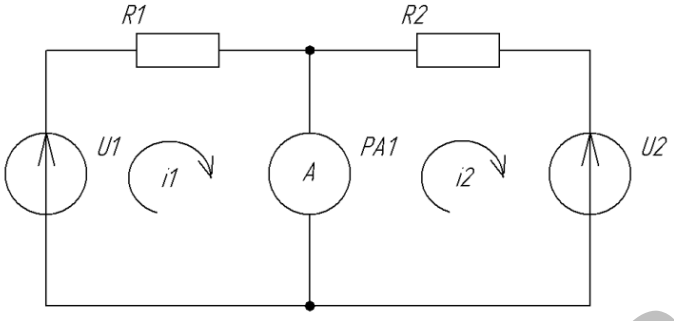

Fig.2. Equivalent circuit.

For automatic balancing, you must be able to dynamically modify the amplitude and phase of the signal generator G2 (Figure 1). In view of the complexity of design of the analog signal generator with adjustable parameters, effectively apply digital signal generators. The digital signal generator (hereinafter DSG) consists of three main parts:

- digital circuit that generates the signal samples;
- digital to analog converter.
- interpolation filter.

The advantages of digital signal generator are:

- a small amount of elements on the printed circuit board;
- ease of management parameters of the synthesized signal;
- no tuning elements;
- no temperature drift of frequency and phase of the signal;
- the ability to synchronize the operation of several synthesizers.

Requirements for the DAC chip meter the impedance depends on the required accuracy of measurement and frequency range of the test signal.

In most modern impedance meter, the frequency range of the test signal lies in the range from 10Hz to 100kHz.

For generating a test sinusoidal signal with a frequency of 100 kHz, according to Theorem Kotelnikov is necessary that the sampling frequency of at least 200 kHz. To facilitate the construction of the interpolating filter, select the sampling rate with a margin, and take it equal to 500kHz.

Among modern DAC chips can distinguish AD5541 from Analog Devices. This DAC satisfies all requirements and is relatively easy to use.

For the formation of a sinusoidal test signal must be supplied to the input of the DAC via the serial interface samples sinusoidal test signal with a sampling frequency of 500kHz. Since the measuring circuit must generate two test signal, the digital part of DSG must generate samples of test signals with a frequency of 1 MHz.

Modern FPGAs contain blocks of memory modules, hardware multiplication modules, logic cells, switching lines and blocks of input-output.

When choosing an FPGA should pay attention to parameters such as maximum speed, number of lines IO, the number of internal configurable logic blocks, and the magnitude of the supply voltage logic levels.

The capabilities and performance of most modern FPGAs is overkill for this task, so choose one of the lower models FPGA company Altera EP2C5 family CycloneII [6].

FPGA should perform the following functions:

- forming two test signals in digital form.
- generating and transmitting samples of a digital signal generated by the DAC through the serial interface.
- reception parameters generated signals via the serial data bus.

Formation of test sinusoidal signals to the FPGA can be performed by direct synthesis from the frequency of the clock signal.

Block diagram of the synthesizer is shown in Figure 3.

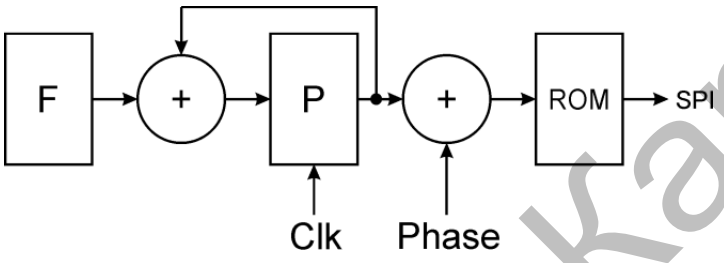

Fig.3. Block diagram of the synthesizer.

In this scheme, P - synchronous register which contains the instantaneous value of the phase of the synthesized signal. The register F is the frequency value, namely the increase phase value of the synthesized signal in one period of the clock signal. In the first adder add up instantaneous value phase and its increment. Result of the addition is latched in the register P. P register value is changed by the action of the front of the clock signal Clk. Thus the output of register P is formed continuously increasing importance of phase. From the second adder is added to the current value of the phase constant "Phase" shift. The signal thus generated is supplied to the address input of the ROM. The memory unit contains one period of samples of sine function. The memory unit contains one period of samples of sine function. Formed samples synthesized signal supplied to the SPI bus, and further, to the DAC. DAC output is generated sinusoidal test signal.

Kernel implementation of digital generator hardware description language Verilog HDL is shown below.

```
module dds(phase,clk,freq,out); //module declaration

input [31:0]phase;          //input value of phase
input [31:0]freq; //input value of frequency
input clk;          //clock signal input
output reg [15:0]out;       //output signal
reg [31:0]akk;              //phase accumulator
reg [15:0]akk_out;          // phase accumulator output
reg [5:0]i;

always @(posedge clk)  //on front of clock signal
begin
   //adder and phase accumulator implementation
   akk <= akk + freq;
   //transfer of phase value to the intermediate register
   for(i = 0; i < 16; i = i + 1)
   begin
```

```
            akk_out[i] = phase[i+16];
    end
    //phase shift
    out = akk_out +  phase;

end
endmodule
```

Figure 4 depicts a module dds as result of compilation above program. The module contains a 32-bit input ports "phase" (to control the phase of the signal) and "Freq" (to control the frequency of the signal) as well as a clock input "clk". On 16-bit block output is generated of linearly increasing phase signal.

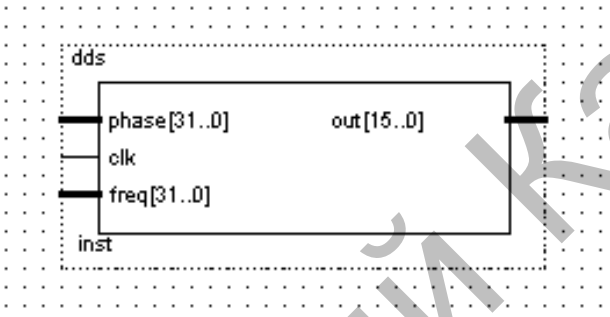

Fig. 4.dds module.

A memory module can be implemented using the Component Wizard (MegaWizard), part of the Quartus II software package. When you create a memory module must specify its basic parameters such as bit data bus, and the bus address.

Serial Interface Module is designed to receive data from the the microcontroller and their separation and write to control registers of DSG. Data received from the microcontroller via a serial line data DIN, clock line SCLK, and select line CS.

Obtained after compiling the module is shown in Figure 5.

The scheme is shown in Figure 6.

The result was a program that allows you to implement on FPGA and high-speed DAC sinusoidal test signal generator with the ability to program adjusting the amplitude, phase and frequency of the test signal.

In operation, the bridge was chosen measuring circuit, chip DAC and FPGA.

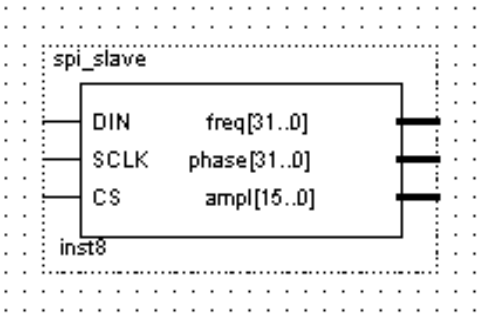

Fig.5. Serial Interface Module.

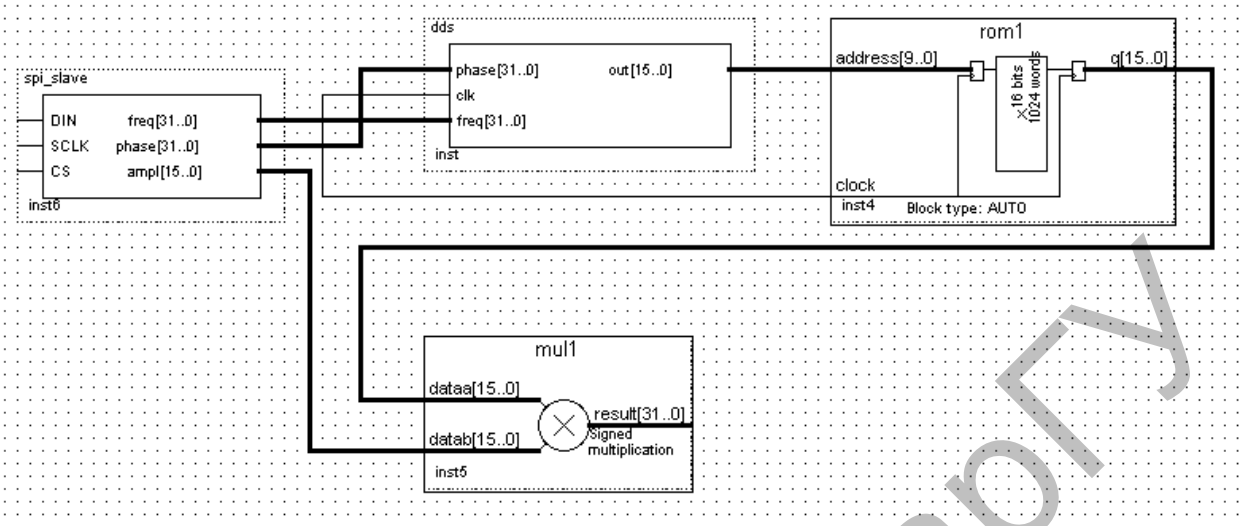

Fig.6.Digital circuit is completed.

The article was selected algorithm of FPGA and implemented using a hardware description language Verilog HDL.

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