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UNIVERSAL MODULAR ONBOARD CONTROL COMPLEX OBCARM G2 NANO FOR NANO-CLASS SPACECRAFT

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Abstract. Universal modular onboard control system OBCARM G2 NANO has been developed for 3U-12U nano-class spacecraft designed for communications, Earth remote sensing, or the Internet of Things. OBCARM G2 NANO consists of interface and processor modules on separate printed circuit boards. The Zynq Ultra scale+ SoC-based processor module provides ARM TMS470-based module telemetry control support and necessary peripherals, including 500 MB DDR4 RAM for the CPU, 125 MB RAM for the programmable logic gate array field-programmable gate array 125 MB QSPI Flash for flight software storing, and 128 GB eMMC Flash as ROM. Interface module contains onboard control system modules power lines, interfaces of the control system and payload data transmitter and receiver, as well as drivers that provide conversion and buffering of payload data. The OBCARM G2 NANO uses QNX RTOS for flight software, and a high-performance AXI bus for interaction between the processor system and field-programmable gate array. CAN bus is used to ensure spacecraft subsystems operation in a single network. The dimensions of the OBCARM G2 NANO mechanical equipment, including a set of temperature monitoring sensors and a thermal bridge for removing excess heat from hot spots, are 95 mm x 95 mm x 35 mm.

Keywords: on-board control complex, field-programmable gate array, processor, interface module, CubeSat.

1. Introduction

Today, the capabilities of small satellites and miniaturized payloads have increased significantly, along with the emergence of new business models based on large-scale low-orbit constellations composed of inexpensive, mass-produced spacecraft (SC). Small satellites typically require lower development and launch costs, making them more accessible to a wide range of organizations and countries. This accessibility has attracted the interest of both commercial companies and academic institutions, allowing them to contribute to space research.

These favorable factors allow all countries to actively participate in SC development and operation. Potential of CubeSats is widely used to accelerate scientific and technological progress in emerging market economies and developing countries. Analytical studies and forecasts indicate that at least 2,000 nano-class SC will be launched into space between 2023 and 2027 [1,2]. OBC, electrical power system (EPS), attitude and orbit control system (AOCS) and communication system are satellite platform fundamental components. At the same time, the choice of onboard control system (OBC) is critical, as it governs the operation of all systems of the SC and payload. When developing OBCARM G2 NANO, the objective was to create a high-performance, compact, versatile OBC capable of meeting the requirements of both low Earth orbit (LEO) communication satellites and CubeSat format remote sensing satellites. The design was based on a previous

version of the NANO model [3,4]. The OBCARM model was modernized taking into account the following requirements:

- development object miniaturization in accordance with the requirements and trends in the spacecraft and electronic systems design principles development [4];
- form factor and mechanical components unification, in accordance with the established standards of the global space community [5];
- increased performance by using field programmable gate arrays (FPGA) in addition to the central processing unit (CPU), either as a standalone unit or as part of a system-on-chip [6-9];
- modeling of operational processes at all stages of development to identify errors before board production, in accordance with industry-specific guidelines [10].

2. OBCARM G2 NANO Architecture

OBCARM G2 NANO consists of two modules - interface and processor, presented on separate printed circuit boards. Processor module (PM) contains the central processor responsible for executing onboard software (FSW), a service node that performs the functions of monitoring and controlling the module, RAM and ROM memory chips, as well as an FPGA for task-specific functionality. Processor module has a connector for interfacing with a radio module used for transmitting payload information and SC telemetry. Interface module includes power distribution across OBCARM G2 NANO modules, as well as a set of interfaces of various standards for communication with the satellite components.

OBCARM G2 NANO modular structure was chosen to achieve a unified and flexible OBC. Commercial OBCs are usually presented as a single solid module containing both external interfaces and processing units, with the possibility of purchasing additional mechanical equipment or a carrier board. However, such designs offer limited flexibility, and any modification or turnkey production significantly increase financial and project costs. Selected processor module based on a 16-layer printed circuit board [3] underwent minimal changes. Main changes were made to the software and FPGA configurations. Processor module is connected to the interface board via two 150-pin connectors and allows duplicating the control of AOCs.

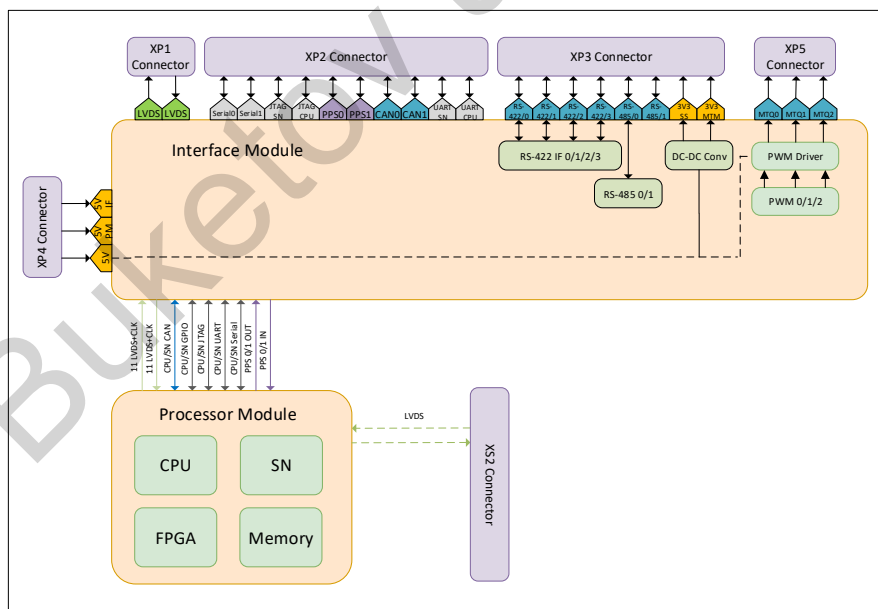


Fig.1. OBC general block-diagram

Interface module is designed on a 6-layer printed circuit board. In case of changes in project requirements or integration into other platforms, OBCARM G2 NANO can be redesigned through the interface module, ensuring its versatility. Unlike most similar solutions on the market, OBCARM G2 NANO offers significantly higher computing power. General block diagram of the OBCARM G2 NANO is shown in Figure 1. The processor module is based on the Zynq UltraScale+ EG series chip. Computing segment of the ZU9EG chipset combines 4 ARM Cortex™-A53 processors with a frequency up to 1.3 GHz to support

L2 cache, as well as 2 Cortex-R5 processors with a frequency up to 533 MHz. XCZU9EG-2FFVB1156I microcircuit supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L memory, with high-speed interfaces such as PCIE Gen2, USB3.0, SATA 3.1, DisplayPort. as well as USB2.0, Gigabit Ethernet, SD / SDIO, I2C, CAN, UART, GPIO. The authors of the work [11,12] showed that Zynq UltraScale+ of the EG series are reliable in operation and implementation of fault mitigation systems. Radiation tolerance test of processors built on crystals of this series showed good results [13,14]. FPGA segment contains an array of programmable logic blocks, digital signal processing (DSP) and internal RAM. FPGA configurability allows flexible configuration of required intellectual property (IP) blocks within the system on a chip without affecting the hardware of processor module. For service node functions implementation microcontroller TMS 470 is used, which is resistant to external factors [15] and performs the following functions:

- Operating current, voltage and temperature of hot spots of the OBCARM G2 NANO monitoring. To ensure these tasks, 12 channels of the microcontroller with ADC for data collection are used;
- OBC components and CPU power supply power-on switching sequence control, ensuring correct initialization and eliminating a number of possible failures;
- CPU power activation, redundant hardware delay and voltage converter enable circuit, which is triggered if TMS is not enabled during platform initialization;
- CPU watchdog timer generates a pulse every minute and, in the event of a malfunction, the service controller will take action according to the embedded algorithms and fault Detection, isolation, and recovery (FDIR) actions;
- restoring the operation of OBCARM G2 NANO and its reconfiguration in case of emergency situations;
- CPU software image loading control;
- providing emergency telemetry.

Processor module uses 4 DDR4 Micron DDR4 MT40A512M16GE memory chips connected to the processor segment (PS), which are combined into a common 64-bit data bus with a capacity of 4 GB. One DDR4 MT40A256M16LY chip with a capacity of 512 MB is connected to the FPGA lines. DDR4 SDRAM on the PS and programmable logic (PL) side maximum operating speed is 1200 MHz (data transfer rate 2400 Mbit/s).

For non-volatile memory, a 128 GB eMMC Flash is used (two 64 GB chips connected in parallel), along with two 64 MB QSPI Flash chips for storing the boot image. The main interfaces of the processor module are 4 ERM8-075-08.0-S-DV-K-TR board-to-board connectors, two of which are located on the front side, two on the back. The front side is used for connection to the interface module, and the back side is intended for connection to the radio module with the corresponding pins. Interface module converts and buffers signal and power interfaces of processor module. Interface module uses 4 five-pin connectors for connection to external systems. List of interfaces is given in Table 1.

Table 1. OBC interfaces configuration.

#	Interface	Signal type	Protocol	Quantity	Max data rate per 1 interface
1	CAN	LVDS(3V3)	NSP	4	500 kbits
2	RS-422	Diff.pair(3V3)	UART	4	10 Mbits
3	RS-485	Diff.pair(3V3)	UART	2	10 Mbits
4	LVDS I/O	LVDS(3V3)	Serial+Clock	32	100 Mbits
5	SERIAL	LVDS(3V3)	Own development	4	1 Mbits
6	PPS	LVDS(3V3)	-	4	1 Hz
7	GTH	LVDS(1V2)	Serial+Clock	4	6.25 Gbits
8	UART	LVC MOS(3V3)	Own development	4	115.2 kbits
9	SPI	LVC MOS(3V3)	SPI	2	25 Mbits
10	I2C	LVC MOS(3V3)	I2C	2	100 kbits
11	JTAG	LVC MOS(3V3)	JTAG	2	115.2 kbits
12	PWM output	0 - +5v -5v - 0v	-	3	-
13	Analog Input	0-3.3V	-	5	-

The listed interfaces can be changed depending on the mission without redesigning OBC complex elements. The functionality of the interfaces is presented in Table 2.

Table 2. Interfaces functionality.

Interface	Processor module connection	Purpose
1	CAN CPU and SN main and redundant CAN I/O	CPU and Service node connection to the main platform data bus
2	RS-422 FPGA configurable I/O	Subsystem elements connection, TM/TS
3	RS-485 FPGA configurable I/O	Subsystem elements connection, TM/TS
4	LVDS I/O FPGA configurable I/O	High-speed, reliable data connection, focused on communication system and payload connection
5	SERIAL FPGA configurable I/O and SN serial I/O	TM/TS Tx/Rx, ground debugging
6	PPS FPGA configurable I/O	Synchronization signal
7	GTH CPU multigigabit transceivers I/O	High-speed, reliable data connection, focused on communication system and payload connection
8	UART FPGA configurable I/O and SN serial I/O	Ground debugging
9	SPI CPU main and redundant SPI I/O	Additional peripherals connection
10	I2C CPU and SN I2C I/O	Redundant data bus
11	JTAG CPU and SN JTAG I/O	Ground debugging
12	PWM FPGA configurable I/O	Magnetorquers (MTQ) control
13	Analog input FPGA configurable I/O	ADC inputs of the interface module for connecting external analog sensors

3. Functional simulation

Electrical circuit simulations were conducted using LTspice and Altium Designer CAD environments. Figure 2 presents the results of the MTQ control simulation, Figures 3,4 show signal integrity in Altium Designer CAD. The main purpose of using LTspice is to simulate the power section and PWM drivers for MTQ control. This simulation is essential for considering the electrical operating parameters when designing the printed circuit board (PCB).

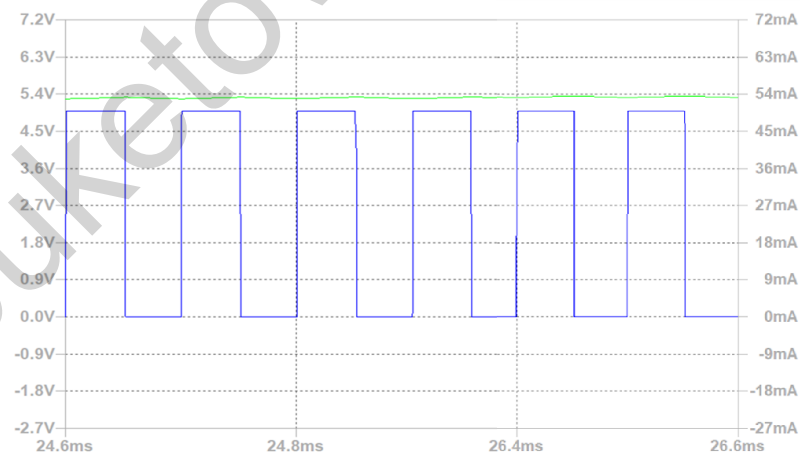


Fig. 2. MTQ control simulation in LTSpice:
Green line – MTQ coil output current, blue line – PWM control signal

Signal integrity simulation was performed to evaluate line termination and line coupling. This analysis was performed after completing the main PCB layout to evaluate performance and reliability, and identify potential issues before the manufacturing stage. Figure 4 shows the reflected signal amplitude in one of the output interfaces microstrip lines measured at 30 μ V. Based on the data in Figure 3, it can be concluded that the line has the correct termination and ensuring that the transmitted signal will not experience significant degradation.

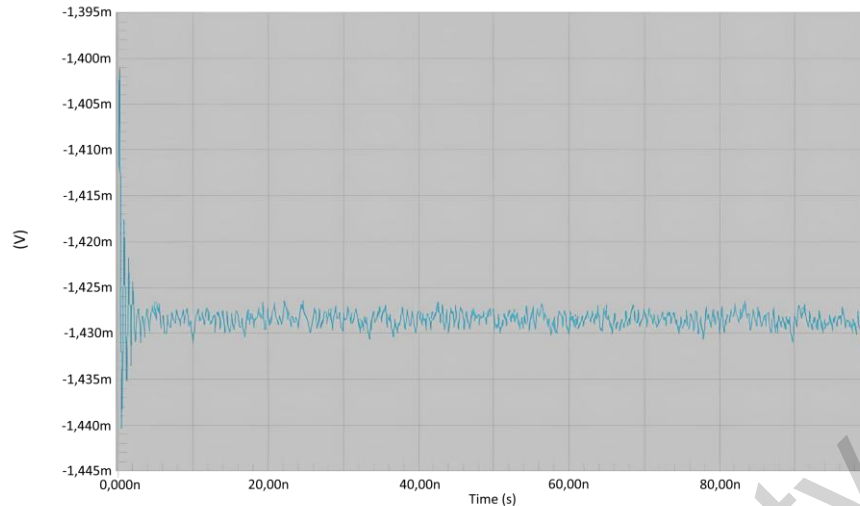


Fig. 3. Reflected signal values in one of output interface microstrip lines with 30 μV amplitude.

Figure 4 shows crosstalk values between two microstrip lines, where A is the shape and magnitude of the signal on the active line, B shows the induced signal on the passive line. With an active upper level of 5 V and the highest frequency component of 166 MHz, the value of the induced interference on the adjacent line does not exceed 2 mV, which is 0.04% of the maximum value and does not pose a threat to the integrity of the signal. Simulation data allow us to conclude that the OBCARM G2 NANO design is carried out in accordance with OBC requirements.

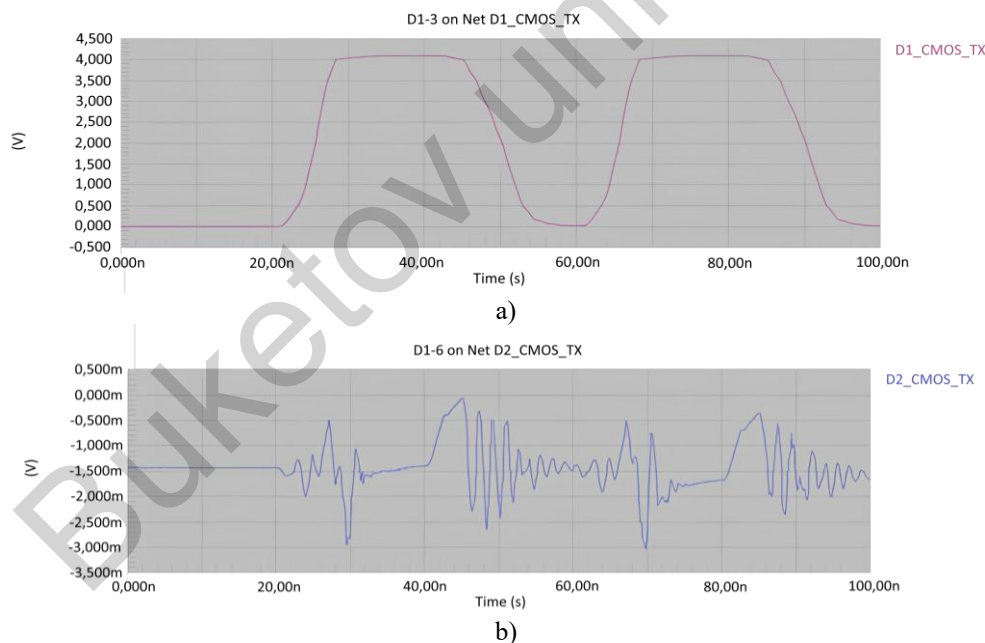


Fig. 4. Crosstalk value between two adjacent microstrip lines:

a) - shape and magnitude of the signal on the active line, b) - shape and magnitude of the signal on the passive line.

4. OBC-Payload interaction

The OBC communicates with payload via three types of signal interfaces:

- Service channel using the RS-422 transmission standard and MODBUS protocol for transmitting TM/TC;
- Data link using the LVDS transmission standard and SpaceWire protocol for transmitting image data from an optical payload.

– Series of 3.3V logic-level signals transmit basic information about the state of the payload (power_ok – the state of the payload power supply, ready – readiness to take a photo) and control the main functions (enable/RST – the backlight and reset signal, trigger – the signal that activates shooting).

Optical payload information is initially saved in its own memory. Upon receiving a command from the OBC, this data is transferred to the FPGA (programmable logic) portion of the system. Images received on the FPGA are saved in OBC permanent memory. Then, according to the communication session schedule, these images are sent to the S-transmitter, which forms a data signal for the ground segment. Data transmission via the OBC is guided by the project's modular and universal design approach, which ensures that replacing the payload or transmitter requires only minimal redesign of the overall platform. In addition, payload and communication system direct connection possibility also remains available. Described interaction block diagram is shown in Figure 5.

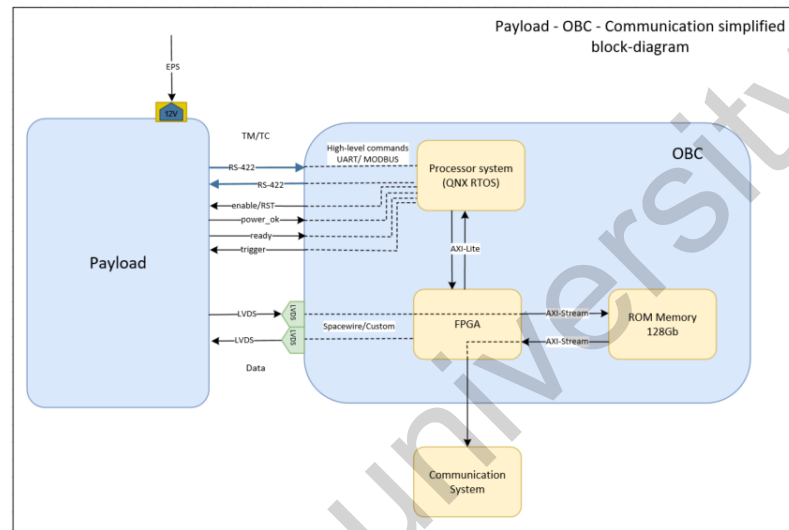


Fig. 5. OBC and payload interaction block-diagram.

5. FPGA architecture

Since the OBC combines a processor system for high-level software operation and programmable logic, it is necessary to develop an architecture for both systems. It was decided to attribute the FPGA architecture to the hardware part. Software architecture is described in the corresponding document. FPGA general architecture design is shown in Figure 6.

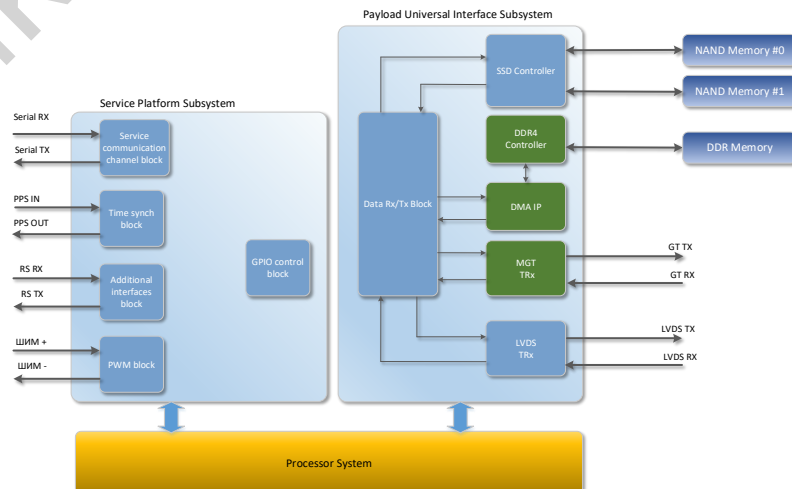


Fig. 6. FPGA general structure block diagram.

FPGA architecture can be divided into two large independent blocks that interact with the processor system via internal AXI bus. Processor system containing high-level software, controls the operation of FPGA blocks where required. Fast and reliable FPGA processes input and output data, removing the potential load from on-board software.

6. Service platform subsystem

The service platform subsystem is designed to receive and transmit telecommands, telemetry and control signals to systems located outside the processor. Service platform subsystem is shown in Figure 7. Its primary components include:

- Service Communication Channel Block: Interfaces with the transceiver, generates compatible protocols, transmits processor-generated telecommands, and decodes received signals.
- Payload Communication Unit: Acts as a backup channel to the optical payload using the Space Packet protocol, enabling command transmission.
- GPIO Control Unit: Generates simple digital control signals (e.g., ENABLE, RESET) for peripheral devices.
- Time Synchronization Unit: Synchronizes onboard time with Global Positioning System (GPS) using a Pulse-Per-Second (PPS) signal for timing of data exchange.
- PWM Generator: Provides adjustable PWM signals for MTQ control when applicable.
- RS-485 and RS-422 Buffers: Translate signals from legacy interfaces to AXI-compatible formats for the processor.

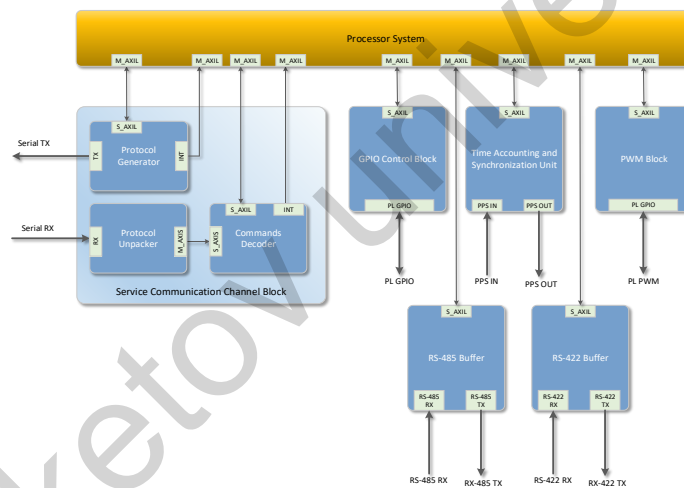


Fig. 7. Service platform subsystem block diagram

7. Universal Interface Subsystem

Universal interface subsystem is designed to form a transmission or reception with minimal redesign effort. Without changing the main configuration, only two IP blocks are requiring changes when adapting to different payload types: LVDS receiver and LVDS transmitter. Block diagram is shown in Figure 8.

- MGT transmitter/receiver blocks: are unused in the current implementation, their presence allows future integration of a custom radio module.
 - LVDS Blocks: Handle protocol formation and decomposition, interfacing directly with payloads. These units are the object of redesign when payload type changes.
 - Reception/Transmission Module: Operates using AXI protocol; routes data to/from ROM, RAM, or directly to communication channels. Includes its own FPGA-based RAM buffer.
 - SSD Controller: Manages read/write operations on two NAND eMMC ROM chips.
 - DMA and DDR4 Controller: Transfer data between memory and interface blocks with minimal processor intervention.
- DMA, DDR4 controller, and MGT transmitter/receiver blocks are require configuration.

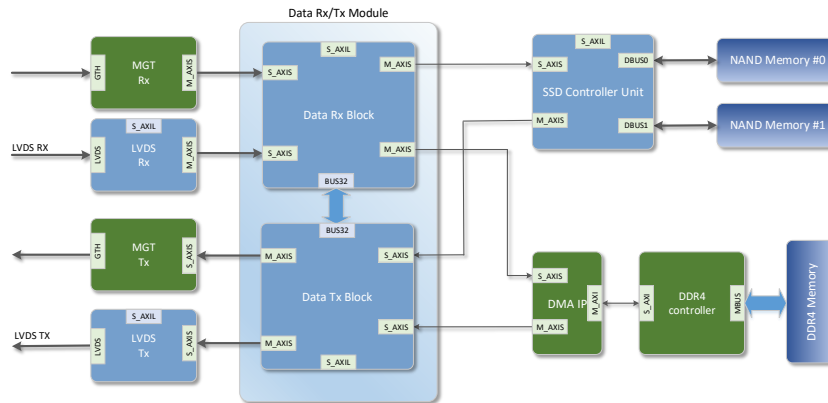


Fig. 8. Universal interface block diagram

8. Comparison of OBCARM G2 NANO with Existing analogues

During preliminary development, existing onboard computer systems were analyzed for benchmarking. Key comparisons are listed below:

- SpaceCube v3 Mini [16] uses previous generation memory, DDR3, and also replaces system-on-a-chip with separate FPGA modules, presented by Kintex Ultrascale and a processor system based on RT proASIC3. OBC has the ability to be installed into a motherboard, to which other modules of this developer can be connected. The breadth of use, comparable computing power is negated when it is necessary to obtain only OBC itself, and the gap in the processor system and FPGA excludes fast data exchange between them. Moreover, external drivers are still necessary to connect interfaces of different types. Considering all the parameters, it is an example of an excellently executed OBC technology.

- Many solutions, for example, the one specified in [17] suggest using the Zynq 7000 system-on-a-chip, which is significantly inferior in performance to the Zynq Ultrascale+, binds AOCS elements control only to OBC, while the OBCARM G2 NANO has the ability to work with AOCS computer as AOCS signals repeater. Also, the analog under consideration uses Linux and I2C as the main communication line.

- Sirius OBC [18], a commercial OBC, offers a robust solution with 64 MB of RAM, 50 MHz processors, and a 5-year orbital life. This OBC handles telemetry and stores payload data, but is not capable of combining the functions of a platform OBC and AOCS OBC.

- NanoMind A3200 [19], another commercial solution, with a larger amount of memory compared to [18], as well as the ability to control AOCS elements. NanoMind A3200 has extremely small dimensions, but will either require additional mechanical equipment for mounting in the platform, or the purchase of a motherboard for subsystems from the same manufacturer. A comparison brief summary is given in Table 3.

Table 3. Comparison of OBCARM G2 NANO and analogous systems

Parameter	OBCARM G2 NANO	SpaceCube v3 Mini [16]	Sirius OBC [18]	NanoMind A3200 [19]
CPU	Zynq Ultrascale+	RT proASIC3	32-bit LEON3FT	AVR32 MCU
FPGA	Zynq Ultrascale+	Kintex Ultrascale	-	-
RAM	500 MB DDR4 – CPU; 125 MB DDR4 - FPGA	2 GB DDR3 – ПЛИС;	64 MB	32 MB
ROM	128 MB QSPI Flash– FSW; 128 GB NAND Flash - ROM	16 Гб NAND Flash – FSW; 16 Гб NAND Flash – ROM;	2 Гб Flash- ROM	128 Мб NOR Flash - ROM
Mass	260 g	-	130 g	24 g
Dimensions	95mm x 95mm x 35mm	95mm x 95mm x 95mm (motherboard included)	95mm x 90mmx 17mm	65mm x 40mm x 7.1mm
Integration difficulty	Low	Medium	Low	Low
AOCS OBC functions	Yes	No	No	Yes
Power	10 W/25 W max.	31 W	1.3 W	3.3 W max

9. Conclusion

The OBCARM G2 NANO is a versatile and modular onboard computer subsystem suitable for a wide range of space missions. Its separation of computational and integration components streamlines platform adaptation and scalability. Using a powerful system-on-a-chip allows execution of complex algorithms for high-performance platforms while remaining energy efficient for smaller spacecraft.

The project has resulted in a multifunctional, fault-tolerant computing solution with straightforward integration procedures, extensive computational resources, and a robust software framework. The OBCARM G2 NANO's modular and mechanically simple design ensures ease of installation across different satellite volumes. Although tailored to the CubeSat form factor, its specifications and flexibility make it equally viable for larger spacecraft platforms.

Conflict of interest statement

The authors declare that they have no conflict of interest in relation to this research, whether financial, personal, authorship or otherwise, that could affect the research and its results presented in this paper.

Credit Author Statement

Sarsenbayev Y.: Concept, Supervision, Architecture Development, Project administration; **Ostretsov K.:** Hardware Development, Hardware Simulation, Writing – Original Draft, Investigation, Resources; **Baktybekov K. (Corresponding Author):** Review & Editing, Validation, Resources. **Mussina A.:** Software Development, Review & Editing; **Yskak A.:** Software Development, Review & Editing;

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